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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10078732	FILING DATE 02/19/2002	CLASS 716	SUBCLASS 8	GAU 2825	EXAMINER TAT
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**APPLICANTS: Tseng Kenneth;

**CONTINUING DATA VERIFIED: BT

** FOREIGN APPLICATIONS VERIFIED: BT

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		07716P001
Verified and Acknowledged Examiner's Initials BT		
TITLE : Variable stage ratio buffer insertion for noise optimization in a logic network		
U.S. DEPT. OF COMM./PAT. & TM-PTO-435L (Rev. 12-94)		

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NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
PREPARED FOR ISSUE		Application Examiner	
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